Docket No.: 278942US40PCT

OBLON SPIVAK

ATTORNEYS AT LAW

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

RE: Application Serial No.: 10/551,439
Applicants: Shinobu KATO
Filing Date: September 29, 2005
For: MULTILAYER PRINTED WIRING BOARD
Group Art Unit: 2841
Examiner: I. B. PATEL

SIR:

Attached hereto for filing are the following papers:

Appeal Brief

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Respectfully submitted,

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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:
SHINOBU KATO	: EXAMINER: I. B. PATEL
SERIAL NO: 10/551,439	:
FILED: SEPTEMBER 29, 2005	: GROUP ART UNIT: 2841
FOR: MULTILAYER PRINTED WIRING BOARD	:

APPEAL BRIEF

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

This is an appeal from a final Office Action mailed February 20, 2009. A Notice of Appeal was timely filed on August 17, 2009.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is IBIDEN CO., LTD., 1, Kandacho 2-chome, Ogaki-shi, Gifu, Japan 503-8604.

II. RELATED APPEALS AND INTERFERENCES

Appellants, Appellants' legal representative and the assignees are aware of no appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS

Claims 1-2, 4-17 are pending, Claims 1, 2, 4-6, 8, 9 and 11-17 stand rejected and are herein appealed. Claims 7 and 10 are withdrawn from consideration by the examiner and Claim 3 is canceled.

IV. STATUS OF THE AMENDMENTS

An Amendment after final rejection was filed on August 17, 2009, which was entered for purposes of Appeal. No other Amendments were filed thereafter. The attached Appendix VIII reflects Claims 1-2, 4-17 as presently pending on appeal.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Claim 1 is directed to a multi-layer printed wiring board including a core substrate (see, for example, page 21, lines 19-30 and items 12, 16E and 16 P of Fig. 8) having a plurality of through holes therein (see, for example, page 25, line 22-page 27, line 15 and items 36S, 36P and 36E of Fig. 8). The through holes in the core substrate are disposed so that a ground through hole (see, for example, page 25, line 22-page 27, line 15 and item 36E in Fig. 8) and a power through hole (see, for example, page 25, line 22-page 27, line 15 and item 36P in Fig. 8) adjoin each other. A distance between the ground through hole and the power through hole is in a range of 60 to 550 μm (see, for example, page 6, lines 5-10 and page 39, lines 6-11). Also included is an interlayer insulating layer formed on the core substrate (see, for example, page 21, lines 19-30 and items 50 and 150) and a conductive layer formed on the interlayer insulating layer(shown in Fig. 8 on the surface of each of items 50 and 150). A plurality of via holes (see, for example, page 21, lines 19-30 and items 60, 160 in Fig. 8) is provided in the insulating layer and configured to provide electrical connection between the conductive layer and through holes.

Claim 16 recites that the core substrate is so constructed that the thick conductive layer as an inner layer comprises first and second thick conductive layers (see, for example, page 21, lines 19-30 and items 12, 16E and 16 P of Fig. 8). These thick conductive layers are formed on respective sides of a metallic plate, which is electrically insulated by a resin layer (item 12 and 14 of Fig. 8, for example). Also, the conductive layer as a surface layer (item 34 of Fig. 8, for example) is formed outside the conductive layer as an inner layer interposed by a resin layer.

Claim 17 recites that the core substrate is so constructed that the thick conductive layer is disposed as the inner layer (items 16E or 16P of Fig. 8, for example) and a thin conductive layer (items 34 of Fig. 8, for example) is formed as the surface layer disposed on a surface side.

VI. GROUNDS FOR REJECTION TO BE REVIEWED ON APPEAL

The following grounds of rejection are presented for review in this Appeal:

A. Claims 16 and 17 stand rejected under 35 U.S.C. § 112, second paragraph;

B. Claims 1, 2, 4, 5, 6 and 11-13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. 6,333,857 to Kanbe et al.

VII. ARGUMENTS

A. Claims 16 and 17 are not indefinite under 35 U.S.C. § 112, second paragraph:

Claims 16 and 17 recite further limitations to the thick conductive layer as an inner layer, which was introduced in intervening Claim 12. As noted in the Summary of Claimed Subject Matter above, an example structure covered by Claims 16 and 17 is shown in Fig. 8 of Appellants specification. This figure shows a metallic plate having a resin layer, a thick conductive layer, another resin layer and a surface conductive layer sequentially formed on

the metal plate. This sequentially layered structure is formed on both side of the metal plate in Fig. 8.

Appellants note that it is settled law that a claim is not indefinite if it apprises one of ordinary skill in the art of the claim's scope even if the claim could be written more clearly using different language.[1] Appellants submit that the scope of Claims 15 and 16 can easily be understood by one of ordinary skill in the art, especially when read in light of the specification, including Fig. 8.

B. Claims 1, 2, 4, 5, 6 and 11-13 are not obvious over Kanbe et al.:

As discussed in Appellants' specification, an IC chip utilizing high switching frequency (for example 5GHz) is prone to switching errors. However, when loop inductance of the printed circuit board for mounting the IC chip is lower than 60pH, IC chip errors can be reduced. Based on this fact, the present inventor determined a relationship between loop inductance and distance between ground and power through holes, and discovered that a distance between ground and power through holes of 60 to 550 μm can provide desired loop inductance and therefore reduce switching errors, even at high switching speeds of 3Ghz or more. This is discussed throughout Appellants' specification, and data relating to experiments performed by the inventors is shown in Fig. 16 of Appellants' specification.[2]

Claim 1 recites that a distance between the ground through hole and the power through hole is in a range of 60 to 550 μm. The Final Office Action admits that Kanbe et al. does not disclose this feature, but states

> . . . the distance will be decided based on the space available in the board to avoid shorting of the adjacent pad on via during operation as well as better routing of the traces.[3]

Further, the Office Action states that

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[1] See MPEP § 2173 generally.
[2] Applicant's specification at pages 3, lines 16-19 and page 6, lines 5-10.
[3] Final Office Action at paragraph linking pages 3-4.

> [T]here are various criteria for maintaining distance between the via holes. One of the criteria is to keep a distance to avoid shorting of the adjacent pad on via during operation or during solder connection or to help better routing of the traces. Use of laminated capacitor does not exclude other criteria to be met.[4]

Applicants respectfully submit that this does not present a *prima facie* case of obviousness.

In particular, cited prior art must either disclose a distance range which overlaps the claimed range, or disclose the distance as a variable which effects the result of that the claimed range is directed to. The Final Office Action admits that Kanbe et al. does not disclose anything about the distance between through holes. Thus, Kanabe et al. does not disclose either a range of distances between through holes which overlaps the claimed range, or that such distance is a variable for effecting any result.

Further, even assuming that the distance between power and ground through holes is a known variable as the Office Action suggests, and that one of ordinary skill in the art would set this distance based on "various criteria," the claimed range would still not be obtained. Specifically, optimization of the distance to satisfy "various criteria" would result in a range of distances between power and ground through holes which optimizes *the selected criteria*. This resulting range would not necessarily overlap, touch or even approach the specific range recited in the claims because this claimed range was selected to mitigate high frequency problems related to power delivery in a printed wiring board. Thus, the Office Action has not presented a *prima facie* case of obviousness.

Moreover, Appellants submit that, in fact, it would not be obvious for one of ordinary skill in the art to modify Kanbe et al. to arrive at the claimed range of distance. Specifically, there are good reasons why one of ordinary skill in the art would not modify the through-hole distances in Kanbe et al. to arrive at the claimed range.

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[4] Final Office Action at Response to Arguments portion, page 8.

First, Kanbe et al. discloses a printed wiring board having a laminated capacitor consisting of composite dielectric layers and metal layers alternately laminated. A first set of metal layers electrically connected to form a first electrode of the capacitor is connected to a first through-hole, while a second set of metal layers electrically connected to form a second electrode of the capacitor is connected to a second through-hole. The first through-hole and first electrode are connected to ground, while the second through-hole and electrode are connected to power.

Thus, in Kanbe et al., the laminated capacitor is parallel inserted between the power source voltage and the land voltage such that noise can be suppressed. That is, Kanbe et al. utilizes the laminated capacitor in the core substrate to solve the problem of noise or delay of power supply to the IC chip which causes switch errors. Therefore, there is no need in Kanbe et al. to provide the claimed distance range between the power and ground through holes for addressing the noise or delay problem because such problem does not exist with the capacitor inserted therein.

Further, one of ordinary skill in the art would not use the through hole distance design of the present invention instead of the capacitor solution in Kanbe et al.. As noted in Kanbe et al., another purpose of the capacitor is to allow checking the character and short-circuit of the laminated capacitor alone as a means of checking the core substrate to prevent further processing of defective core substrates. That is, the laminated capacitor makes it possible to check only the core substrate (rather than the further processed circuit board) so that a yield rate can be improved. Eliminating the capacitor and addressing the delay and noise problem with through hole spacing would also render Kanbe et al. unfit for this reduced yield purpose.

Finally, reducing the distance between the power and ground through holes in Kanbe et al. is contrary to the purpose of the laminated capacitor itself. As noted in Kanbe et al., the capacitance is preferably large in order to mitigate the signal delay and noise problems.

Since Kanbe et al. forms a laminated capacitor in the core substrate by an area of the metal layer between adjacent through holes, if the distance between the through holes is reduced, an effective area of the capacitor electrode would be reduced. This would create a problem of reduced capacitance in Kanbe et al. That is, a modification of Kanabe et al. to include the claimed distance would provide structure which is unfit for the intended purpose of Kanbe et al., i.e., to provide a relatively large capacitance for addressing the noise and delay problems stated in Kanbe et al.

In summary, Appellants submit that one of ordinary skill in the art would never imagine, from the Kanabe et al. reference, the idea that narrowing the pitch of the through holes can obtain the effect of cancellation of the induced electromotive force occurring in the ground through holes and the power through holes. Thus, Claim 1 is not obvious over Kanbe et al.

Stadberg does not show the distance or placement of the ground through hole and the power through hole. Therefore, Stadberg cannot correct the deficiencies of Kanbe et al.

CONCLUSION

For the reasons discussed above, all pending claims patentably define over the cited references. Therefore, the rejection should be reversed.

Respectfully submitted,

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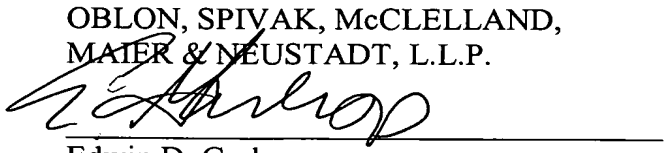

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VIII. CLAIMS APPENDIX

Claim 1: A multi-layer printed wiring board comprising:

a core substrate having a plurality of through holes therein, the through holes in the core substrate being disposed so that a ground through hole and a power through hole adjoin each other, wherein a distance between the ground through hole and the power through hole is in a range of 60 to 550 μm;

an interlayer insulating layer formed on the core substrate;

a conductive layer formed on the interlayer insulating layer; and

a plurality of via holes provided in the insulating layer and configured to provide electrical connection between the conductive layer and through holes.

Claim 2: The multi-layer printed wiring board according to claim 1, wherein the ground through hole in the core substrate including two or more ground through holes and the power through hole including two or more power through holes, such that the ground through holes and the power through holes are disposed in a grid formation or in a staggered formation at adjacent positions.

Claim 4: The multi-layer printed wiring board according to -claim 1, wherein the diameter of the ground through hole is 50 to 500 μm and the diameter of the power through hole is 50 to 500 μm.

Claim 5: The multi-layer printed wiring board according to claim 1, wherein at least one through hole of the ground through holes and the power through holes comprises two or more through holes -in a stack structure through all layers of the multi-layer printed wiring board up to an outermost layer.

Claim 6: The multi-layer printed wiring board according to any one of claims 1, 2 or 5 wherein the ground through hole and the power through hole are disposed just below an IC chip.

Claim 7: The multi-layer printed wiring board according to claim 1 or 2 wherein the thickness of conductive layer on the core substrate is larger than the thickness of the conductive layer on the interlayer insulating layer.

Claim 8: The multi-layer printed wiring board according to claim 1 or 2 wherein assuming that the thickness of the conductive layer on the core substrate is α 1 and the thickness of the conductive layer on the interlayer insulating layer is $\alpha 2$, $\alpha 2 < \alpha 1 \leqq 40\alpha 2$.

Claim 9: The multi-layer printed wiring board according to claim 8 wherein the $\alpha 1$ is in a relation of $1.2\alpha 2 \leqq \alpha 1 \leqq 40\alpha 2$.

Claim 10: The multi-layer printed wiring board according to -claim 7, wherein each conductive layer of the core substrate is conductive layer for power layer or conductive layer for grounding.

Claim 11: The multi-layer printed wiring board according to -claim 1, wherein a capacitor is mounted on the surface thereof.

Claim 12: The multi-layer printed wiring board according to claim 1 or 2 wherein the core substrate is a multi-layer core substrate composed of three or more layers and including a thick conductive layer as an inner layer, and a conductive layer as a surface layer, and

the conductive layer of each inner layer of the core substrate and the conductive layer of each surface layer are a conductive layer for power layer or a conductive layer for grounding.

Claim 13: The multi-layer printed wiring board according to claim 1 or 2 wherein the core substrate is a multi-layer core substrate composed of three layers and including a thick conductive layer as an inner layer, and

the conductive layer of each inner layer of the core substrate is conductive layer for power layer or conductive layer for grounding and the conductive layer on the front surface side is composed of signal line.

Claim 14: The multi-layer printed wiring board according to claim 12, wherein the thickness of the conductive layer of the inner layer of the core substrate is larger than the thickness of the conductive layer on the interlayer insulating layer.

Claim 15: The multi-layer printed wiring board according to claim 12 or 13 wherein the conductive layer in the inner layer of the core substrate is composed of two or more layers.

Claim 16: The multi-layer printed wiring board according to claim 12, wherein:

the core substrate is so constructed that the thick conductive layer as an inner layer comprises first and second thick conductive layers formed on respective sides of a metallic

plate which is electrically insulated by a resin layer, and the conductive layer as a surface layer is formed outside the conductive layer as an inner layer interposed by a resin layer.

Claim 17: The multi-layer printed wiring board according to claim 12, wherein the core substrate is so constructed that the thick conductive layer is disposed as the inner layer and a thin conductive layer is formed as the surface layer disposed on a surface side.

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.

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